Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-24 (cancelled)

Claim 25 (previously presented) A method of programming a laser programmable integrated circuit, comprising:

providing an alignment structure on the integrated circuit, the alignment structure formed using a planarized process, the alignment structure comprising a substrate, a first region formed on the substrate, and a second region formed on the substrate adjacent to the first region, the first region characterized by a first optical reflectiveness value and the second region characterized by a second optical reflectiveness value different from the first optical reflectiveness value;

aligning the integrated circuit using the alignment structure;

referencing a first programmable element located on the integrated circuit using a laser; and

programming the first programmable element using the laser.

Claim 26 (previously presented) The method of claim 25 wherein the integrated circuit is a programmable logic device (PLD) comprising a plurality of logical elements and a plurality of interconnections between the logical elements.

Claim 27 (previously presented) The method of claim 26 wherein programming the first programmable element using the laser comprises configuring a logical element from the plurality of logical elements using the laser.

Claim 28 (previously presented) The method of claim 26 wherein programming the first programmable element using the laser comprises configuring an interconnection from the plurality of interconnections using the laser.

Claim 29 (previously presented) The method of claim 25 wherein the programmable element is a fuse, an antifuse, an EPROM, a flash, an EEPROM, or a SRAM cell.

Claim 30 (previously presented) The method of claim 25 further comprising:

programming a second programmable element located on the integrated circuit using in-system programming.

Claim 31 (previously presented) The method of claim 25 wherein the second region of the alignment structure comprises:

a first conductive layer;

a second conductive layer formed above the first conductive layer,

an first insulating layer, between the first and second conductive layers, wherein the first insulating layer has a first opening for electrically coupling the first and second conductive layers; and

a plug layer filling the first opening, wherein the first plug layer has a cored region, whereby a topographical roughness formed by the cored region scatters incident radiation.

Claim 32 (previously presented) The method of claim 31 wherein the second region of the alignment structure further comprises:

a third conductive layer formed above the second conductive layer; and

a second insulating layer, between the second and third conductive layers, wherein the second conductive layer has a second opening, stacked above the first opening, for electrically coupling the third and second conductive layers, whereby the second opening aggravates the topographical roughness formed by the cored region.

Claim 33 (previously presented) The method of claim 25 wherein the second region of the alignment structure comprises:

a contact opening formed on the substrate; and

a first plug layer filling the contact opening, the first plug layer having a first depressed region in the contact opening, whereby a topographical roughness formed by the first depressed region scatters incident radiation.

Claim 34 (previously presented) The method of claim 33 wherein the second region of the alignment structure further comprises:

a first via opening stacked on top of the contact opening, whereby the first via opening enhances the topographical roughness formed by the first depressed region.

Claim 35 (previously presented) The method of claim 34 wherein the second region of the alignment structure further comprises:

a second via opening stacked on top of the first via opening and second via opening, whereby the second via opening further enhances the topographical roughness.

Claim 36 (previously presented) The method of claim 25 wherein:

the first region comprises a first portion and a second portion, wherein the first portion of the first region is perpendicular to the second portion of the first region; and

the second region comprises a first portion and a second portion, wherein the first portion of the second region is adjacent to the first portion of the first region, and the second portion of the second region is adjacent to the second portion of the first region.

Claim 37 (previously presented) A method of programming a laser programmable integrated circuit, comprising:

providing an alignment structure on the integrated circuit, the alignment structure formed in a planarized semiconductor process, the alignment structure comprising:

a substrate;

a first region formed on the substrate, the first region characterized by a first optical reflectiveness value; and

a second region formed on the substrate adjacent to the first region, the second region characterized by a second optical reflectiveness value different from the first optical reflectiveness value, the second region comprising:

a first conductive layer;

a second conductive layer;

an first insulating layer, between the first and second conductive layers, wherein the first insulating layer has a first opening for electrically coupling the first and second conductive layers; and

a plug layer filling the first opening, wherein the first plug layer has a cored region, whereby a topographical roughness formed by the cored region scatters incident radiation.;

aligning the integrated circuit using the alignment structure;

referencing a first programmable element located on the integrated circuit using a laser; and

programming the first programmable element using the laser.

Claim 38 (previously presented) A method of programming a programmable logic integrated circuit comprising:

aligning the programmable logic integrated circuit, fabricated using a planarized process, using a laser to scan a plurality of alignment structures formed on the integrated circuit, wherein each alignment structure in the plurality of alignment structures comprises:

a first region formed on a substrate of the integrated circuit, the first region characterized by a first optical reflectiveness value; and

a second region formed on the substrate adjacent to the first region, the second region characterized by a second optical reflectiveness value different from the first optical reflectiveness value; and

programming a first programmable element of the programmable logic integrated circuit using the laser.

Claim 39 (previously presented) The method of claim 38 wherein the first programmable element is a fuse.

Claim 40 (previously presented) The method of claim 38 wherein the second region of each alignment structure comprises:

a first conductive layer;

a second conductive layer formed above the first conductive layer,

an first insulating layer, between the first and second conductive layers, wherein the first insulating layer has a first opening for electrically coupling the first and second conductive layers; and

a plug layer filling the first opening, wherein the first plug layer has a cored region, whereby a topographical roughness formed by the cored region scatters incident radiation.

Claim 41 (previously presented) The method of claim 40 wherein the second region of each alignment structure further comprises:

a third conductive layer formed above the second conductive layer; and

a second insulating layer, between the second and third conductive layers, wherein the second conductive layer has a second opening, stacked above the first opening, for electrically coupling the third and second conductive layers, whereby the second opening aggravates the topographical roughness formed by the cored region.

Claim 42 (previously presented) The method of claim 38 wherein the second region of each alignment structure comprises:

a contact opening formed on the substrate; and

a first plug layer filling the contact opening, the first plug layer having a first depressed region in the contact opening, whereby a topographical roughness formed by the first depressed region scatters incident radiation.

Claim 43 (previously presented) The method of claim 42 wherein the second region of the alignment structure further comprises:

a first via opening stacked on top of the contact opening, whereby the first via opening enhances the topographical roughness formed by the first depressed region.

Claim 44 (previously presented) The method of claim 43 wherein the second region of the alignment structure further comprises:

a second via opening stacked on top of the first via opening and second via opening, whereby the second via opening further enhances the topographical roughness.

Claim 45 (previously presented) The method of claim 38 wherein aligning the programmable logic integrated circuit comprises:

detecting a position of a first alignment structure from the plurality of alignment structures using the laser;

detecting a position of a second alignment structure from the plurality of alignment structures using the laser; and

aligning the programmable logic integrated circuit using the first alignment structure and the second alignment structure.

Claim 46 (previously presented) The method of claim 45 wherein detecting the position of the first alignment structure using the laser comprises:

scanning the first alignment structure using the laser along a line traversing the first region and the second region of the first alignment structure;

detecting a change in reflectivity as the laser scans across the first region and the second region; and

determining the position of the first alignment structure based upon the change in reflectivity.

Claim 47 (previously presented) The method of claim 38 wherein:

the first region comprises a first portion and a second portion, wherein the first portion of the first region is perpendicular to the second portion of the first region; and

the second region comprises a first portion and a second portion, wherein the first portion of the second region is adjacent to the first portion of the first region, and the second portion of the second region is adjacent to the second portion of the first region.

Claim 48 (previously presented) The method of claim 38 wherein each alignment structure from the plurality of alignment structures has a first portion extending in a first direction and a second portion extending in a second direction transverse to the first direction.

Claim 49 (previously presented) The method of claim 38 wherein the first programmable element is used to configure functionality of programmable logic of the integrated circuit.

Claim 50 (previously presented) The method of claim 38 wherein the plurality of alignment structures comprises at least three alignment structures.

Claim 51 (previously presented) The method of claim 38 wherein the first programmable element is used to implement a redundancy scheme of the integrated circuit.

Claim 52 (previously presented) The method of claim 38 wherein aligning the programmable logic integrated circuit comprises:

scanning a first alignment structure from the plurality of alignment structures in a first direction and in a second direction transverse to the first direction.